UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,318	02/27/2004	Belgacem Haba	TESSERA 3.0-331	9218

38091 7590 06/30/2008

TESSERA
LERNER DAVID et al.
600 SOUTH AVENUE WEST
WESTFIELD, NJ 07090

EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
06/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/789,318	HABA, BELGACEM	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-13,16-26,28-33,38-45,47-54 and 56-60* is/are pending in the application.

4a) Of the above claim(s) *47-54 and 56-60* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-13,16-26,28-33 and 38-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 26, 2007, has been entered.

Election/Restrictions

2. Applicant's election without traverse of Species I, in the reply filed on April 21, 2008, is acknowledged. Claims 1-9, 11-13, 16-26, 28-33 read on the elected species.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-5, 8, 9, 11-13, 16-26, 28-30, 32, 33 and 38-45** are rejected under 35 U.S.C. 102(b) as being anticipated by **Suminoe et al. (US 6,380,620, cited in previous Office Action, hereinafter, Suminoe)**.

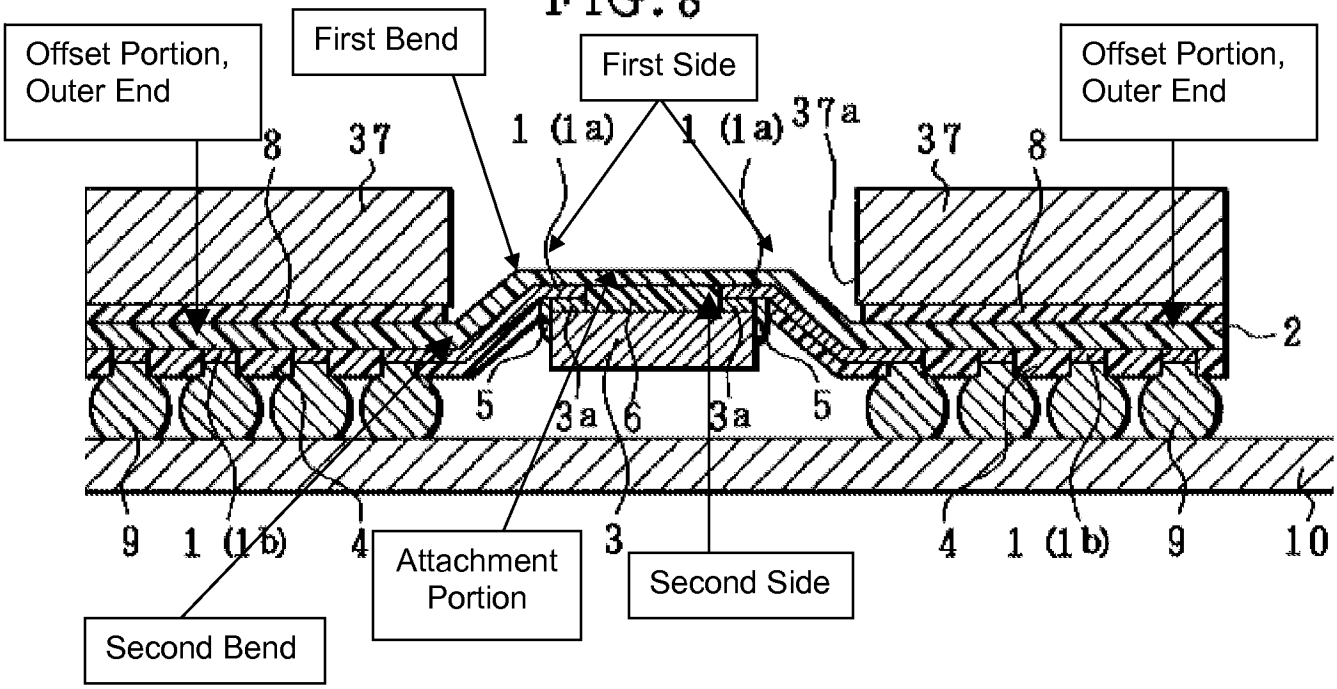
With respect to **claim 1, Suminoe** teaches a microelectronic assembly **(FIG. 8, illustrated below)**, comprising:

a) a dielectric layer **(2)** having an attachment portion **(labeled in FIG. 8 below)**, the dielectric layer **(2)** having a first side **(labeled in FIG. 8 below)** and an oppositely facing second side **(labeled in FIG. 8 below),** the first side of the dielectric layer in the attachment portion facing in a first direction, the second side of the dielectric layer in the attachment portion facing in a second direction, the dielectric layer having at least one offset portion **(labeled in FIG. 8 below)** offset from the attachment portion such that the offset portion is skewed in said second direction as compared to said attachment portion;

b) a semiconductor chip **(3)** assembled to the second side of the dielectric layer in the attachment portion, wherein the first side of the dielectric layer **(2)** defines a boundary of the assembly such that the entire first side is unobstructed **(as shown in FIG. 8 below, the first side of the dielectric layer is exposed)**; and

c) terminal structures **(9)** carried by the offset portion of the dielectric layer **(2)** for connecting the semiconductor chip **(3)** with external circuitry **(10)** lying at a lower level than the attachment portion **(col. 8: lns. 39-65; col. 14: lns. 1-30)**.

FIG. 8



With respect to **claim 2, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the attachment portion **(labeled in FIG. 8 above)** of the dielectric layer **(2)** is substantially planar.

With respect to **claim 3, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **(2)** has at least one bend **(col. 14: lns. 12-14)** between the attachment portion **(labeled in FIG. 8 above)** and the offset portion **(labeled in FIG. 8 above)**.

With respect to **claim 4, Suminoe** teaches the assembly of claim 3 as set forth above, wherein the at least one bend comprises a first bend in the third direction and a second bend **(labeled in FIG. 8 above)** in fourth direction opposite to the third direction.

With respect to **claim 5, Suminoe** teaches the assembly of claims 4 as set forth above, wherein the dielectric layer **(2)** has at least one conductor **(1a, 1b)** extending in the bend **(FIG. 8)**.

With respect to **claim 8, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the offset portion **(labeled in FIG. 8 above)** of the dielectric layer **(2)** extends substantially perpendicular to the second direction away from the semiconductor chip **(3)**.

With respect to **claims 9, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **(2)** has at least one conductor **(1a, 1b)**, arranged so as to shield the semiconductor chip **(3) (FIG. 8)**.

With respect to **claim 11, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the offset portion **(labeled in FIG. 8 above)** of the dielectric layer **(2)** comprises a portion that lies outwardly of the attachment portion **(labeled in FIG. 8 above)** of the dielectric layer.

With respect to **claim 12, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **(2)** has at least one outer end and the terminal structures **(9)** are disposed at the at least one outer end **(FIG. 8)**.

With respect to **claim 13, Suminoe** teaches the assembly of claim 12 as set forth above, wherein the at least one outer end extends substantially horizontally **(FIG. 8)**.

With respect to **claim 16, Suminoe** teaches the assembly of claim 1 as set forth above, further comprising a circuit element **(10)** connected to the terminal structures **(9)** so that the circuit element is disposed underneath the dielectric layer **(2) (FIG. 8)**.

With respect to **claim 17, Suminoe** teaches the assembly of claim 16 as set forth above, wherein the terminal structures **(9)** interconnect the semiconductor chip **(3)** with the circuit element **(10) (FIG. 8)**.

With respect to **claim 18, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **(2)** includes traces **(1a, 1b)** connected to the terminal structures **(9)** and connected to contacts **(3a)** of the semiconductor chip **(3) (FIG. 8)**.

With respect to **claim 19, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the semiconductor chip **(3)** has a first face with contacts **(3a)** exposed at the first face **(FIG. 8)**.

With respect to **claim 20, Suminoe** teaches the assembly of claim 19 as set forth above, wherein the semiconductor chip **(3)** is assembled to the attachment portion so that the first face faces in an upward direction **(chip 3 is face bonded to the attachment portion, FIG. 8 above)**.

With respect to **claim 21, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **(2)** comprises a continuous sheet **(FIG. 8)**.

With respect to **claim 22, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the terminal structures **(9)** comprise bonding material **("solder balls," col. 8, lns. 39-42).**

With respect to **claim 23, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the terminal structures **(9)** are connected to conductors **(1a, 1b)** extending through the attachment portion **(labeled in FIG. 8 above)**.

With respect to **claim 24, Suminoe** teaches the assembly of claim 1 as set forth above, wherein the terminal structures **(9)** comprise solder balls **(col. 5, lns. 49-50).**

With respect to claim 25, Suminoe teaches a microelectronic assembly, comprising:

a) a dielectric layer **(2)** having an attachment portion **(labeled in FIG. 8 above)**, the dielectric layer having a first side, a second side, and outer ends **(all labeled in FIG. 8 above)** lying outwardly of the attachment portion, the outer ends being offset from the attachment portion;

b) a semiconductor chip **(3)** assembled to the second side of the dielectric layer **(2)** at the attachment portion; the entire first side **(labeled in FIG. 8 above)** of the dielectric layer being unobstructed; and

c) terminal structures **(9)** carried by the outer ends of the dielectric layer **(2)** for connecting the semiconductor chip **(3)** with external circuitry **(10) (FIG. 8, as illustrated above; col. 8: lns. 39-65; col. 14: lns. 1-30)**.

With respect to **claim 26, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the attachment portion **(labeled in FIG. 8 above)** of the dielectric layer **(2)** is substantially planar.

With respect to **claim 28, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the dielectric layer **(2)** has at least one bend **(col. 14: lns. 12-14)** between the attachment portion **(labeled in FIG. 8 above)** and the outer ends **(labeled in FIG. 8 above)**.

With respect to **claim 29, Suminoe** teaches the assembly of claim 28 as set forth above, wherein the at least one bend comprises a first bend in a first direction and a second bend **(both labeled in FIG. 8 above)** in second direction opposite to the first direction.

With respect to **claim 30, Suminoe** teaches the assembly of claims 28 as set forth above, wherein the dielectric layer **(2)** has at least one conductor **(1a, 1b)** extending in the bend **(FIG. 8)**.

With respect to **claim 32, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the outer ends **(labeled in FIG. 8 above)** of the dielectric layer **(2)** extend substantially in away from the first side of the attachment portion **(labeled I FIG. 8 above)** of the dielectric layer **(2)**.

With respect to **claim 33, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the outer ends **(labeled in FIG. 8 above)** of the dielectric layer **(2)** extend substantially horizontally.

With respect to **claim 38, Suminoe** teaches the assembly of claim 25 as set forth above, further comprising a circuit element **(10)** connected to the terminal structures **(9)** so that the circuit element is disposed underneath the dielectric layer **(2) (FIG. 8)**.

With respect to **claim 39, Suminoe** teaches the assembly of claim 38 as set forth above, wherein the terminal structures **(9)** interconnect the semiconductor chip **(3)** with the circuit element **(10) (FIG. 8)**.

With respect to **claim 40, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the dielectric layer **(2)** includes traces **(1a, 1b)** connected to the terminal structures **(9)** and connected to contacts **(3a)** of the semiconductor chip **(3) (FIG. 8)**.

With respect to **claim 41, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the semiconductor chip **(3)** has a first face with contacts **(3a)** exposed at the first face **(FIG. 8)**.

With respect to **claim 42, Suminoe** teaches the assembly of claim 41 as set forth above, wherein the semiconductor chip **(3)** is assembled to the attachment portion so that the first face faces in an upward direction **(chip 3 is face bonded to the attachment portion, FIG. 8 above)**.

With respect to **claim 43, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the dielectric layer **(2)** comprises a continuous sheet **(FIG. 8)**.

With respect to **claim 44, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the terminal structures **(9)** comprise bonding material **("solder balls," col. 8, lns. 39-42).**

With respect to **claim 45, Suminoe** teaches the assembly of claim 25 as set forth above, wherein the terminal structures **(9)** are connected to conductors **(1a, 1b)** extending through the attachment portion **(labeled in FIG. 8 above)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 6, 7, and 31** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Suminoe (presented above)**.

With respect to **claims 6 and 31, Suminoe** teaches the microelectronic assembly of claims 1 and 25, respectively, as set forth above, wherein the at least one conductor **(1a, 1b)** extends along the bend of the dielectric layer **(2) (FIG. 8 above)**.

Thus, **Suminoe** teaches all the limitations of claims 6 and 31, with the exception of disclosing: wherein the conductor is arranged to support the bend in the dielectric layer. However, the functional limitation "to support the bend in the dielectric layer," is implicit because **Suminoe's** device has the same structure as applicant's claimed invention.

Furthermore, an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber,* 128 F.3d 1473, 1477-78, 44USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart*, 439 F.2d 210 212-13, 169 USPQ 226, 228-29 (CCPA 1971); *In re Danly*, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).

"Apparatus claims cover what a deivce is, not what a device does." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

With respect to **claim 7, Suminoe** teaches the microelectronic assembly and component of claim 1, as set forth above, wherein the dielectric layer **(2)** comprises a polymeric material **(col. 8: lns. 56-65)** that includes an offset portion **(labeled in FIG. 8 above)**.

Thus, **Suminoe** teaches all the limitations of claim 7, with the exception of disclosing: forming the offset portion by molding the polymeric material. However, the limitation of forming the offset portion by molding the polymeric material, is a product by process limitation and therefore is given no patentable.

Initially, and with respect to claim 7, note that a "product by process" claim is directed to the product per se, no matter how actually made. *In re Thorpe et al.,* 227 USPQ 964, (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product per se which must be determined in a "product by process" claim, and no the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe:

> Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington,* 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935);

Note that Applicant has burden of proof in such cases as the above case law makes it clear.

Response to Arguments

Applicant's arguments, filed July 26, 2007, with respect to claims 1-9, 11-13, 16-26, and 28-33 have been considered but are not persuasive.

Applicant argues that "Suminoe fails to teach that a side of the dielectric layer defines a boundary of the assembly such that the entire first side of the dielectric layer is unobstructed, as required by independent Claims 1 and 25." The argument is not persuasive because the top most side (labeled "first side" in FIG. 8 above) of the dielectric layer **2** reads on Applicant's claimed limitations. Thus, the top most side of the defines a boundary of the assembly such that the entire top most side of the dielectric layer **2** is unobstructed. Note that only the top most side of the dielectric layer **2** is interpreted as the first side of the dielectric layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/A. K./
Examiner, Art Unit 2814

/Phat X Cao/
Primary Examiner, Art Unit 2814